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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/079,775	02/19/2002	Marina V. Plat	D900D/1368D	9123

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EXAMINER	
LEE, HSIEN MING	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/079,775	PLAT ET AL.	
	Examiner	Art Unit	
	Hsien-ming Lee	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 13-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-18* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☒ Claim(s) *4-6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

HSIEN-MING LEE
PRIMARY EXAMINER
Lee
1/4/05

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Grounds of Rejection

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung et al. (US 6,184,142) in view of applicants admitted prior art ("AAPA").

In re claims 1-2, Chung et al., in Figs. 6A-6F and related text, teach the claimed method providing a semiconductor device, the semiconductor including a first layer 113/116/112 desired to be etched, the method comprising the steps of:

(a) providing by depositing an antireflective coating (ARC) layer 114 (Fig. 6A), which is a SiON having antireflective properties (col. 4, lines 30-32);

(b) patterning a first resist layer 130, the first resist layer 130 including a pattern having a singular aperture therein for etching a first portion (i.e. the portion where a dual damascene opening to be formed) of the first layer 113/116/112 (Fig. 6A);

(c) etching the first portion of the first layer 113/116/112 to form a via (Figs. 6C);

(d) removing the first resist layer 130 utilizing a plasma etch with O_2 plasma (Figs. 6A-6B), the ARC being resistant to the plasma etch (see previous office action, page 4, second paragraph);

(e) patterning a second resist layer 131, the resist layer 131 including a pattern having a plurality of apertures therein for etching a second portion of the first layer 113/116/112 (Fig.6D); and

(f) etching the second portion of the first layer 113/116/112 to form a trench as shown in Fig. 6F (Figs. 6E-6F).

Chung et al. do not teach that the first resist layer 130 has a plurality of apertures.

However, AAPA, teaches providing the ARC layer 52 on a polysilicon layer 51; patterning a first resist layer 53, the first resist layer 53 including a pattern having a plurality of apertures therein for etching a first portion of the polysilicon layer 51 to form plural gate stack in a memory region 42 and patterning a second resist layer (step 22 in Fig.1), the second resist layer having a plurality of apertures because it forms plural gates in Logic region (step 24 in Fig.1).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time of the invention was made, to apply the method of Chung et al. to a situation where it needs the plurality of apertures in the resist pattern, as taught by AAPA, since by this manner it would provide a ground for the subsequent processing steps in forming plural gate stack.

As far as the thickness of the ARC layer is concerned, Chung et al. further teach that the ARC layer has a thickness of between about **500** to 1,000 Angstroms (col. 3, lines 46-52). The thickness range "between about 500 to 1,000 Angstroms" allows for thickness slightly less than 500 Angstroms, which obviously teaches the use of a thickness within claimed range "less than about 500 Angstroms." See M.P.E.P. 2144.05 Obviousness of Ranges

In re claim 3, Chung et al. also teach using an oxygen plasma (col. 4, line 47) including a forming gas (i.e. oxygen-containing gas), the ARC layer being resistant to the plasma etch

because Chung et al. suggest a desirability of protecting the low-k dielectric layer from oxygen-plasma etching damage during photoresist layer stripping (col. 1, lines 52-67).

Allowable Subject Matter

3. Claims 13-18 are allowed.

4. Claims 4-6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter: see previous Office Action.

Response to Arguments

6. Applicant's arguments filed 11/1/2004 have been fully considered but they are not persuasive for the reasons as follows.

Applicant argued that the motivation is insufficient to support a *prima facie* case of obviousness. (page 22, fourth and fifth paragraphs)

In response to the argument, a clear motivation (i.e. providing a ground for the subsequent processing steps in forming plural gate stack) has been established, as stated previously. This motivation comes from the source of a *common knowledge of persons of ordinary skill in the art.*

Chung et al. teach a similar method as claimed, comprising patterning a first resist layer 130 to form a pattern having a singular aperture therein (Fig.6A) and patterning a second resist layer 131 to form a pattern having a plurality of apertures (i.e. opening) as shown in Fig.6D, whereas claim 1 recites "the resist layer including a pattern having a plurality of apertures

therein", wherein the resist layer is equivalent to the first resist layer 130 in Chung et al.. In other word, the **only** difference between the teachings of Chung et al. and the instant invention is that the first resist 130 in Chung et al. has a *singular* aperture or opening (Fig. 6A), whereas the first resist layer in the instant invention has *plural* apertures.

To remedy the above deficiency, the teaching of applicant's admitted prior art ("AAPA") is used.

AAPA, in Figs. 3A-3C and related text, demonstrate the steps of providing the *anti-reflective coating layer* 52 on a polysilicon layer 51; patterning a first *resist layer* 53, the first resist layer 53 including a pattern having *a plurality of apertures* therein for etching a first portion of the polysilicon layer 51 to form *plural gate stack* in a memory region 42 and patterning a second resist layer (step 22 in Fig.1), the second resist layer having a plurality of apertures (step 24 in Fig.1). Thus, AAPA and Chung et al. are in the *same endeavor* since both AAPA and Chung et al. teach providing *anti-reflective coating* on the first *resist layer* and *patterning resist layers* to form *apertures* (i.e. openings) therein. By applying the teachings of Chung et al. to AAPA would not destroy the teachings of AAPA but rather it would provide a ground for forming the plural gate stacks, as shown in AAPA.

Therefore, one of the ordinary skill in the art would have been motivated to modify the teachings of Chung et al., without departing the spirit of the teachings (col. 5, lines 1-4, Chung et al.), to the situation where it needs plural apertures as in making plural gate stack, as taught by AAPA. As a result, the obviousness has been clearly and properly established, which does not rely upon Examiner's subjective opinion.

Applicant also argued that "the Examiner's conclusion of obvious is based on improper hindsight reasoning." (second paragraph, page 23).

In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Applicant further argued that Chung et al. do not teach or suggest that the stop layer 114 is resist to a plasma etch. (last paragraph, lines 15-16, page 24)

In this regard, Chung et al. teach that the stop layer 114 also *acts as the anti-reflective coating layer* (i.e. ARC, col. 4, lines 24-25 and 28-31), wherein the ARC is SiON (col. 4. lines 30-32), which is the *same material* as claimed. Having the same material, it would also have an identical characteristic, i.e. resist to the plasma etch.

Applicant argued that 'Chung and Applicants' Background, taken singly or in do not teach or suggest "performing the plasma etch using a plasma including a forming gas, the anti-reflective coating layer being resistant to the plasma etch using the plasma including the forming gas" as recited in claim 3.' (second paragraph, page 25)

In response to the argument, it is submitted that Chung et al teach performing the plasma etch using an oxygen plasma (col. 4, line 47), which inherently comprises an oxygen-containing

gas (i.e. the forming gas). The anti-reflective coating layer, which is SiON, is resist to the oxygen plasma, as stated previously. Thus, the teachings of Chung et al. do read on claim 3.

For the reasons as given, the 103(a) rejection against claims 1-3, as set forth in the previous Office Action, is deemed proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on Tuesday-Thursday (8:00 ~ 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-ming Lee
Primary Examiner
Art Unit 2823

Jan. 4, 2005

HSIEN-MING LEE
PRIMARY EXAMINER

1/4/05